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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,679	12/11/2001	Jeffrey D. Walker	15436.247.45.1	3207

22913 7590 09/21/2004

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EXAMINER	
HELLNER, MARK	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

KM

Office Action Summary	Application No.	Applicant(s)	
	10/014,679	WALKER ET AL.	
	Examiner	Art Unit	
	Mark Hellner	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22 and 24-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for reconsideration of the finality of the rejection of the last Office action and the corresponding amendment to the claims is persuasive and, therefore, the finality of that action is withdrawn.

NEW ACTION

An update search has found new "prior art" and, a such, a new grounds of rejection is presented below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-19 and 24-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verma et al.

Verma et al disclose an integrated optical device (column 4, line 33) comprising: a VLSOA (100); an amplifier input (112); an amplifier output (114); a semiconductor active region (104); an amplifying path connecting the input to the output (130); and a vertical laser cavity (140).

The difference between claim 1 and Verma et al is the addition of an optical element wherein a portion of the VLSOA and optical element are formed on aq common substrate by a common fabrication process an at least one parameter varies between the portion of the VLSOA and a portion of the optical element.

Column 4, lines 33 to 42 of Verma et al teach that their VLSOA can be integrated with optical waveguides or other VLSOAs .

A person of ordinary skill would have been led to the difference in claim 1 pointed out above because a different waveguide or VLSOA would have possessed different parameters.

Claim 2 is taught by Verma et al because a waveguide or other VLSOA would have a different transition energy and selective area epitaxy is taught by column 4, lines 44-52.

Impurity induced disordering (claim 3) is taught by column 4, lines 44-52.

Stress induced disordering (claim 4) is part of standard semiconductor fabrication techniques and, as such, would have been suggested by column 4, line 44.

Claim 5 is taught by column 4, line 35.

A waveguide in the optical art inherently has a core and cladding, thus allowing column 5, line 35 to also teach claim 6. Different transition energies are taught because a waveguide does not amplify and, as such, has no transition energy.

Claims 7-9 are taught by column 4, lines 44-52.

Claim 10 and 11 are taught by column 4, line 41. Transition energies would have been dependent on the amplification level required by the individual VLSOA in the suggested array

Claims 12-14 are taught by column 4, lines 44-52.

An unguided transport region falls into the category of another device and, as such, is suggested by column 4, line 34.

Claim 16 is rejected for the reasons applied to claim 1. A separate fabrication process would have been obvious when the person of ordinary skill in the art was faced with the problem of coupling the VLSOA to another device that would not have been able to have been constructed by the process applicable to the VLSOA.

Claim 17 is taught by column 4, line 50.

Claim 18 is taught for the reasons applied to claim 6.

Claim 19 is taught by the reasons applied to claims 10 and 11.

Claim 24 is rejected for the reasons applied to claim 1.

The fabrication steps set forth by claims 25-31 are known parts of the standard fabrication methods listed by column 4, lines 44-52.

Claims 20-23 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verma et al in view of Yoshimura et al.

Verma et al disclose the structure of claim 24 (see rejection of claim 1) with the exception of forming the optical element and VLSOA on separate substrates by separate fabrication processes and then integrating them on a common subtrate.

Figure 1 of Yoshimura et al teaches separately formed optical IC chips (1a to 1d) that are subsequently placed onto a common substrate (10). Column 11, lines 23-25 teach that the IC chips can be devices that include a VCSEL (the laser cavity of the Verma et al device).

It would have been obvious for a person of ordinary skill in the art to have considered the teaching of Yoshimura et al when seeking to follow the use of an array of VLSOAs suggested by column 4, line 41 of Verma et al.

The Yoshimura et al teaching would have provided a compact integrated structure.

The combination taught above produces claim 20.

Claims 21 and 22 are taught by the OE layer (10) of Yoshimura et al.

Claims 32-34 are taught by Vera et al and Yoshimura et al as applied to claims 20-23.

Any inquiry concerning this communication should be directed to Mark Hellner at telephone number 703 306 4155.

Mark Hellner

Primary Examiner

AU 3663

Mark Hellner